

FIG. 1 PRIOR ART

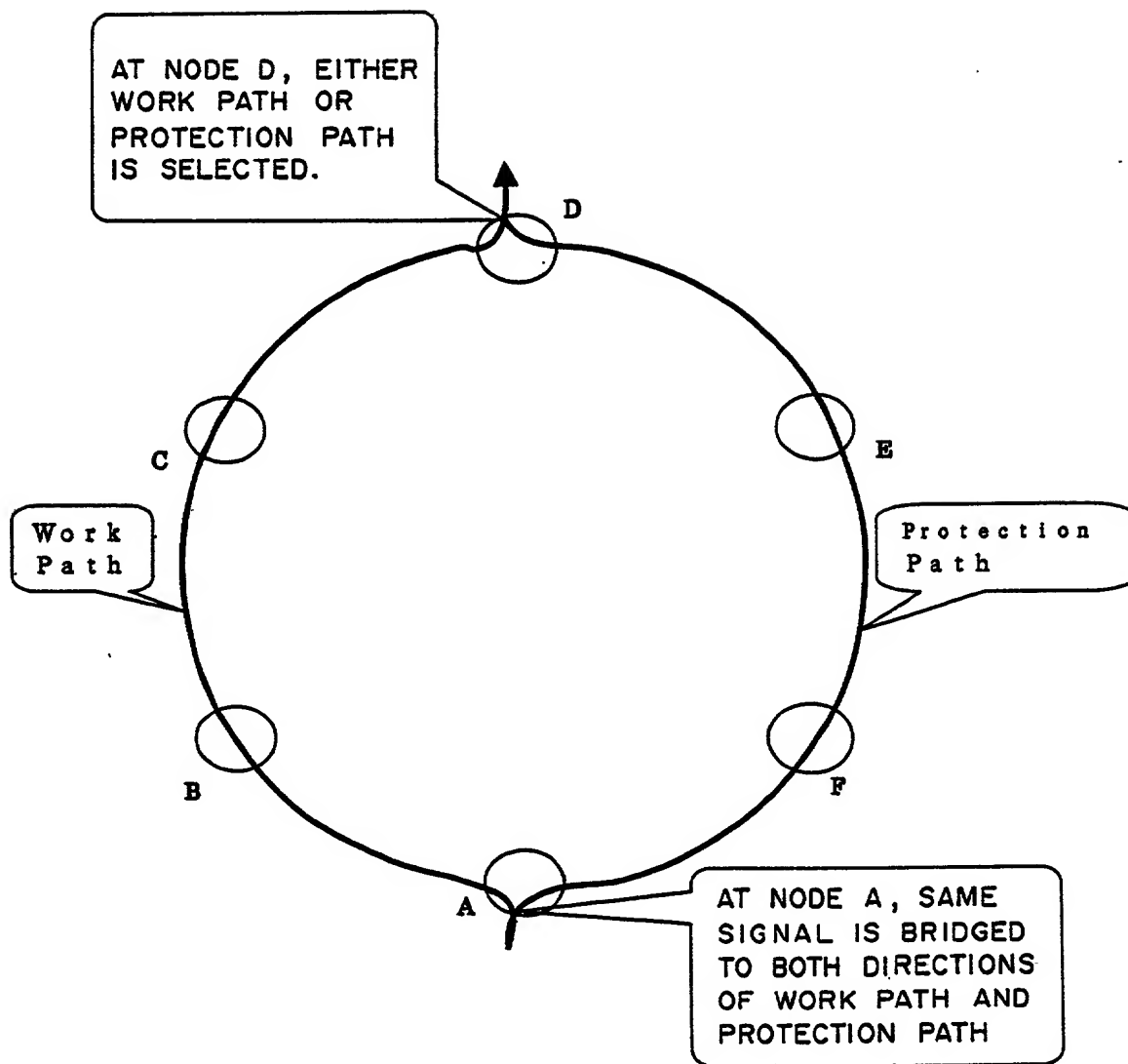


FIG. 2 PRIOR ART

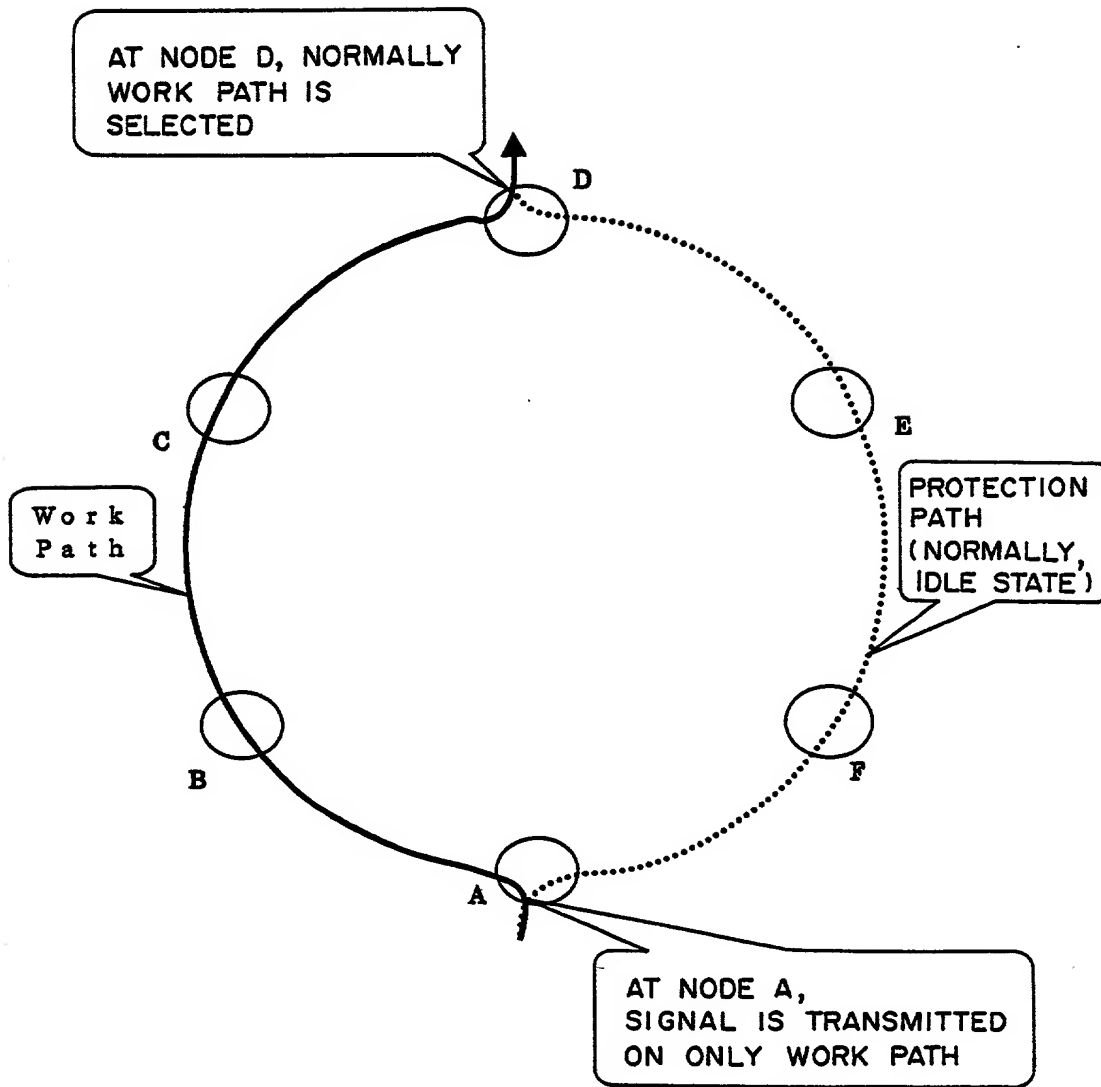


FIG. 3 PRIOR ART

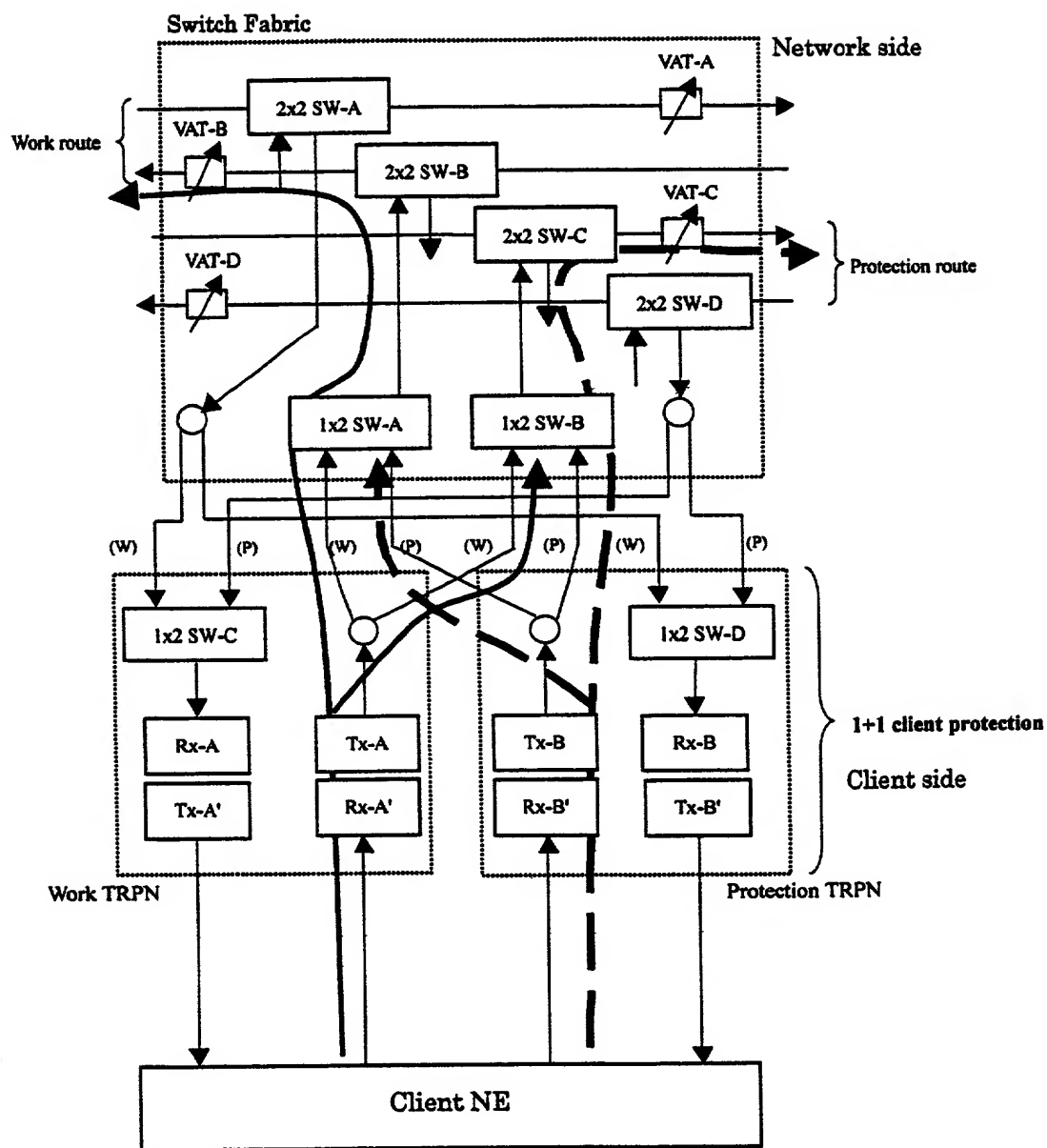


FIG. 4 PRIOR ART

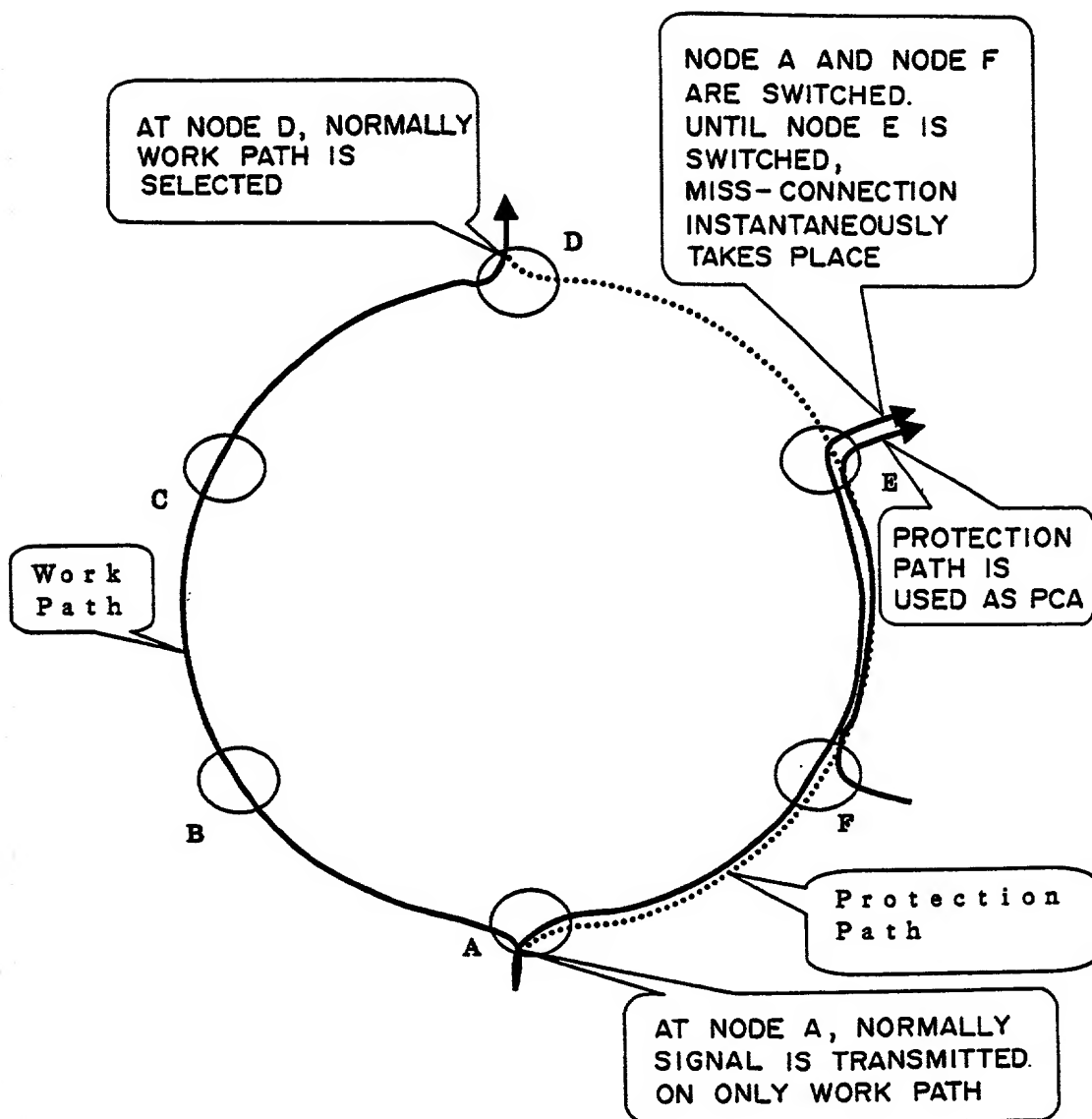
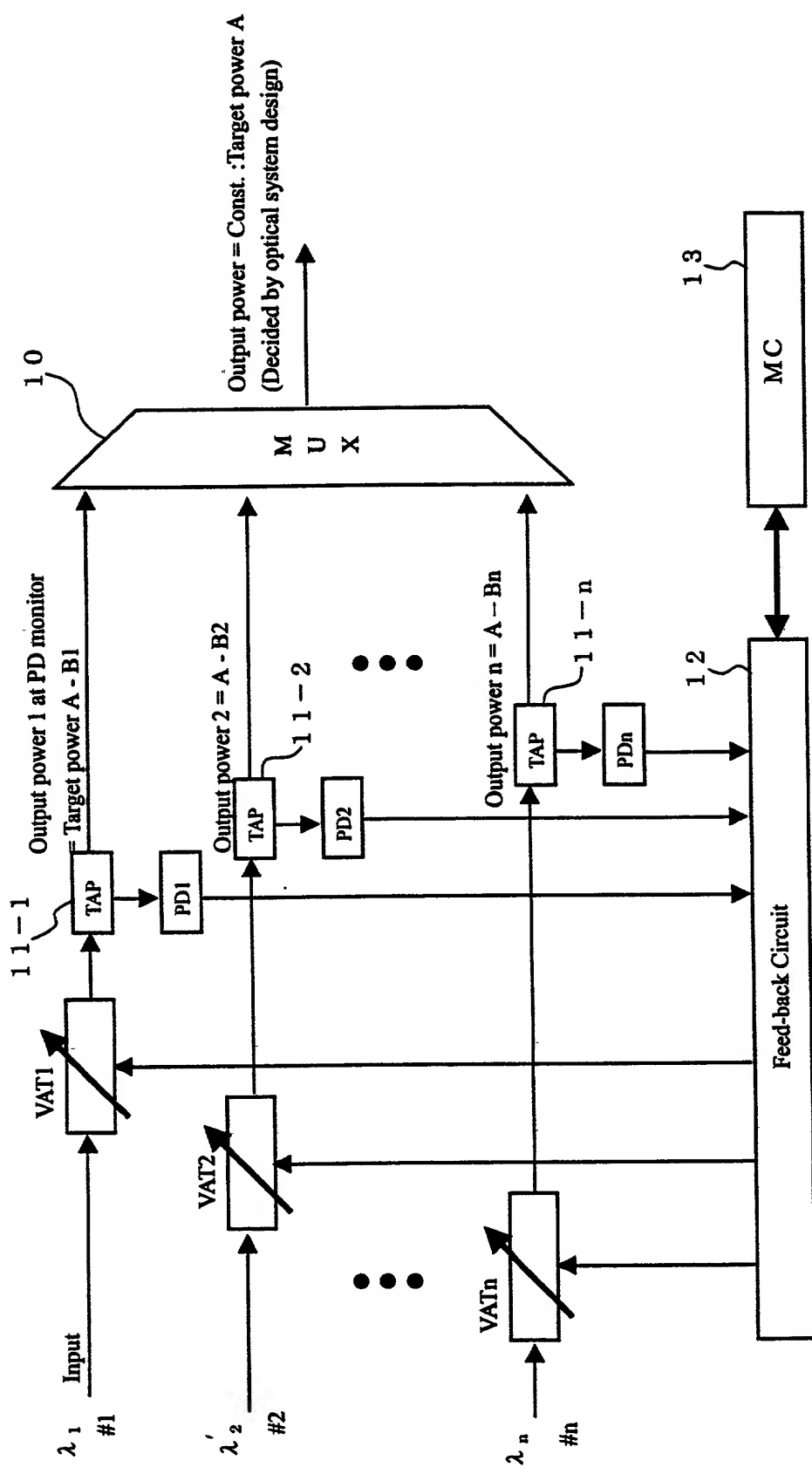


FIG. 5 PRIOR ART



A = Target power at Post Amplifier input

B<sub>x</sub> = Off-set power value

B INCLUDES FLUCTUATION OF LOSSES OF PORTS OF AWG, TAP, AND SPLICE (CONNECTOR) AND MEASUREMENT ERROR OF PD MONITOR.

FIG. 6

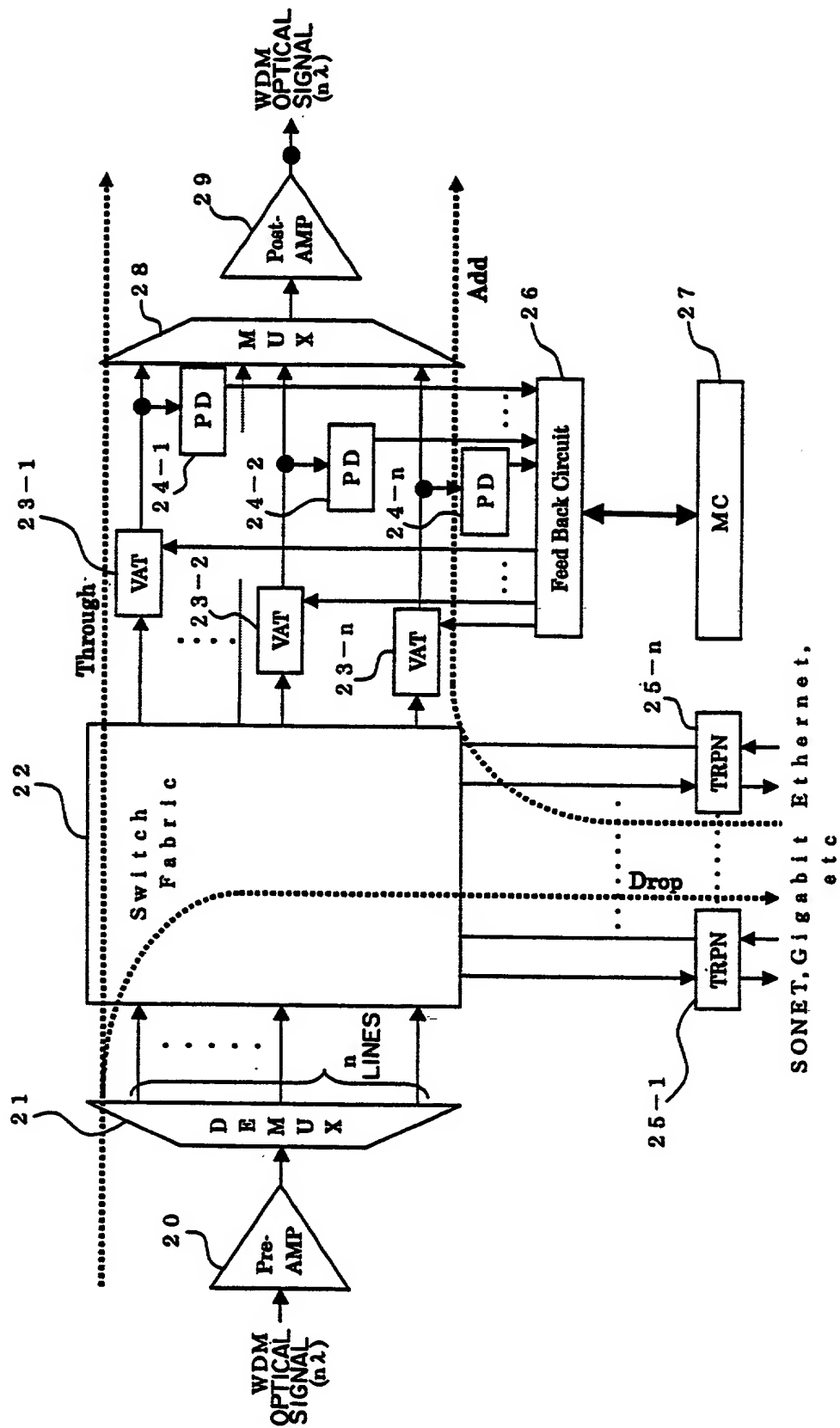


FIG. 7

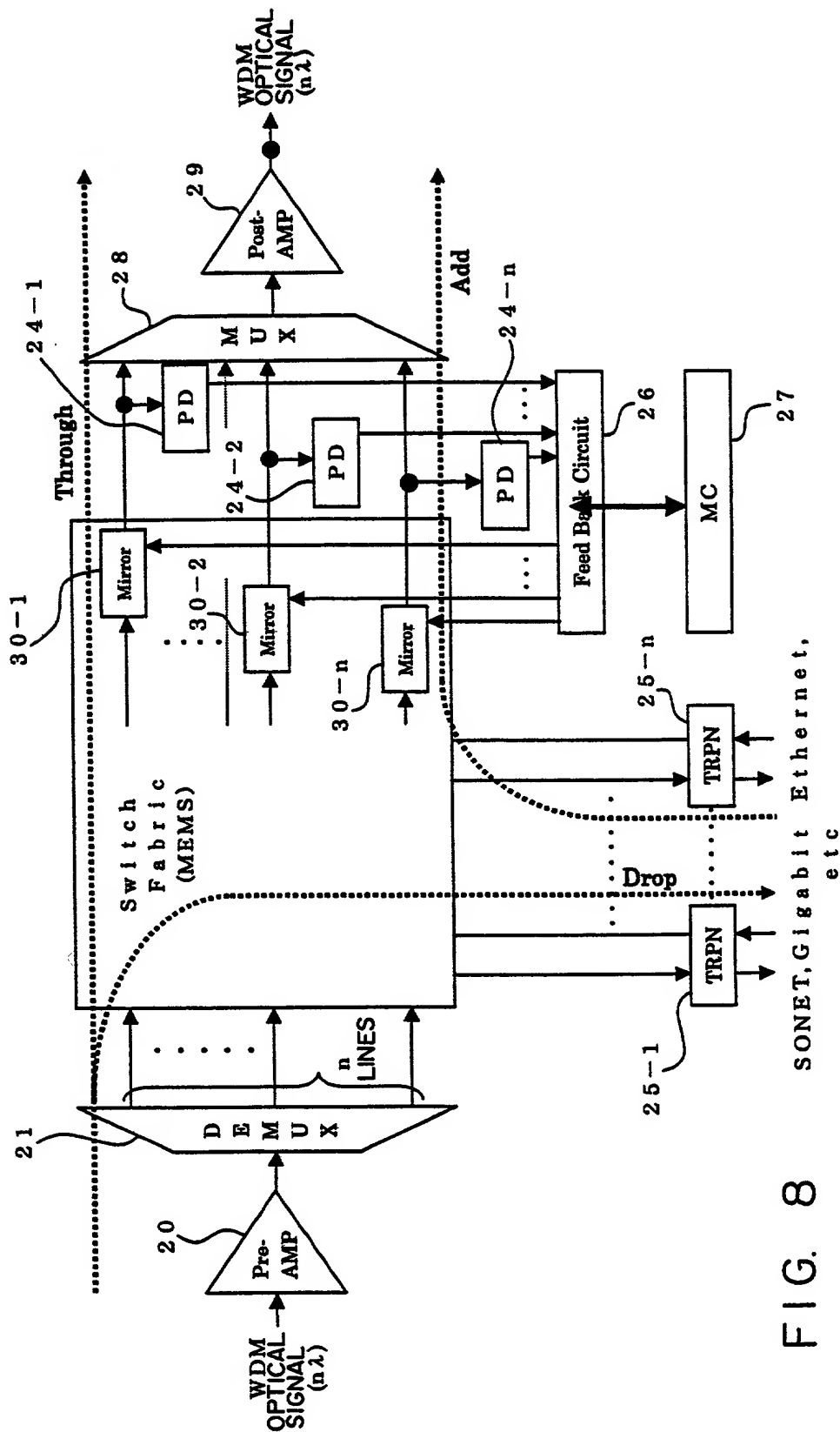


FIG. 8

SONET, Gigabit Ethernet,  
etc



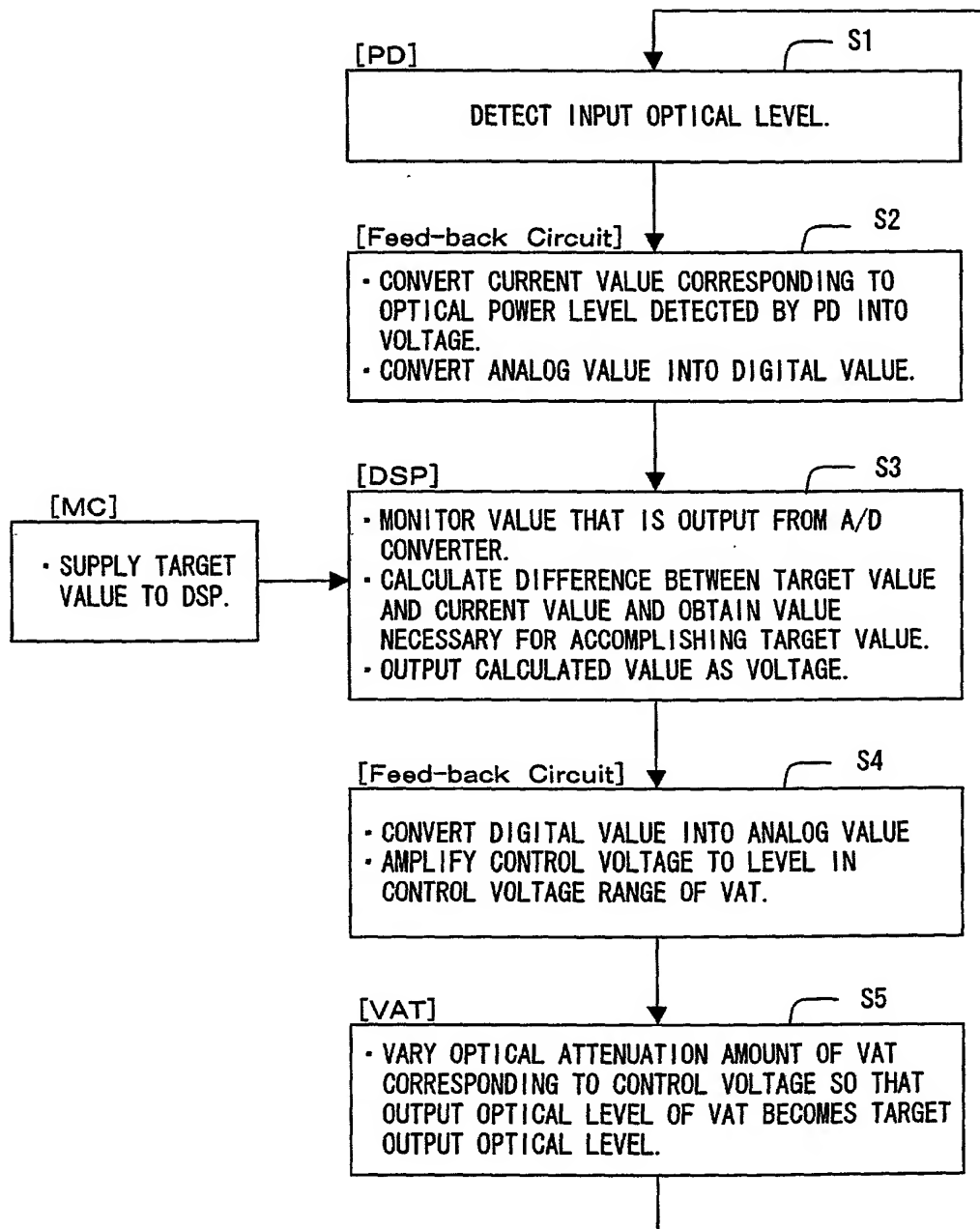


FIG. 9

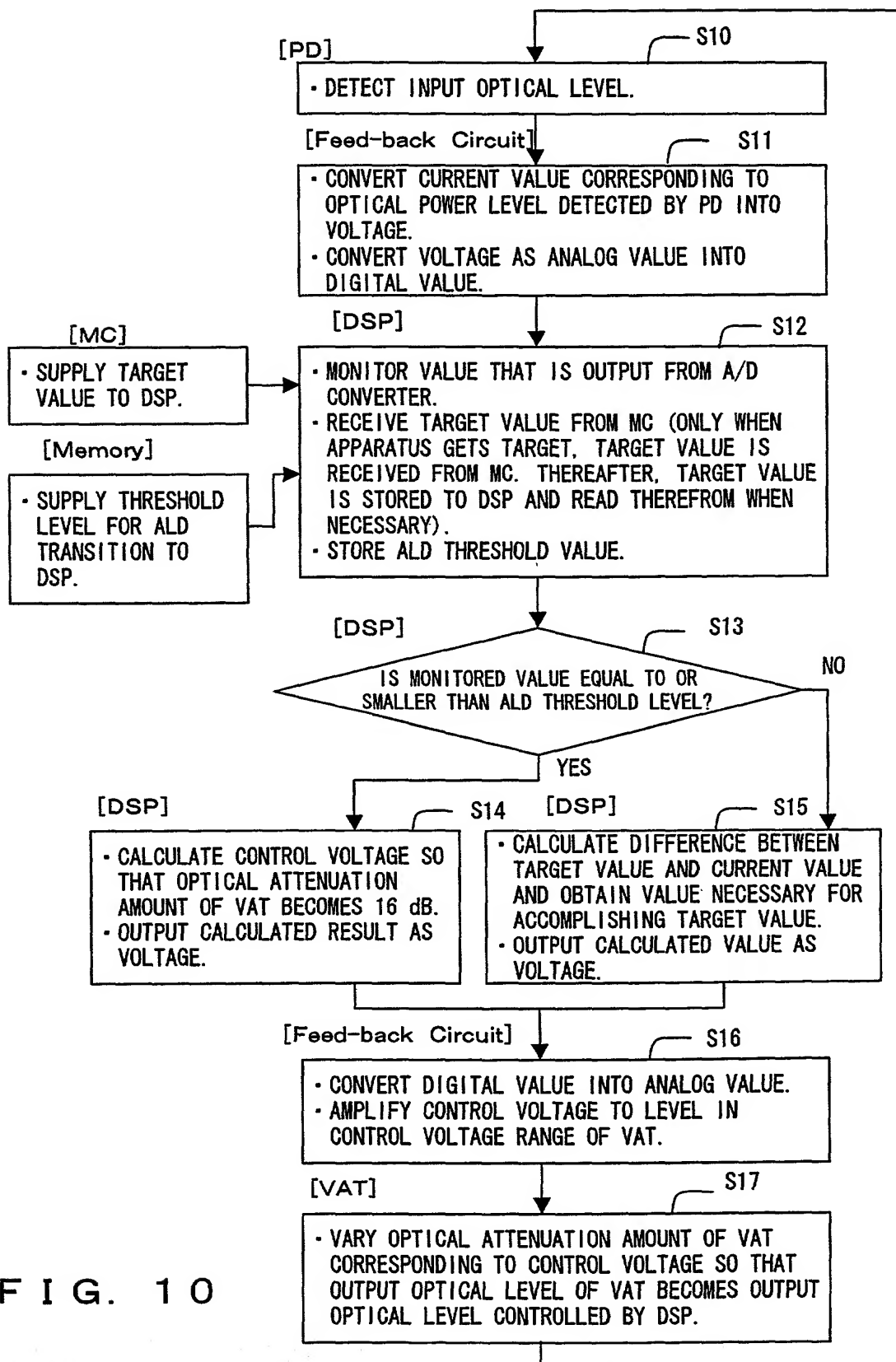


FIG. 10

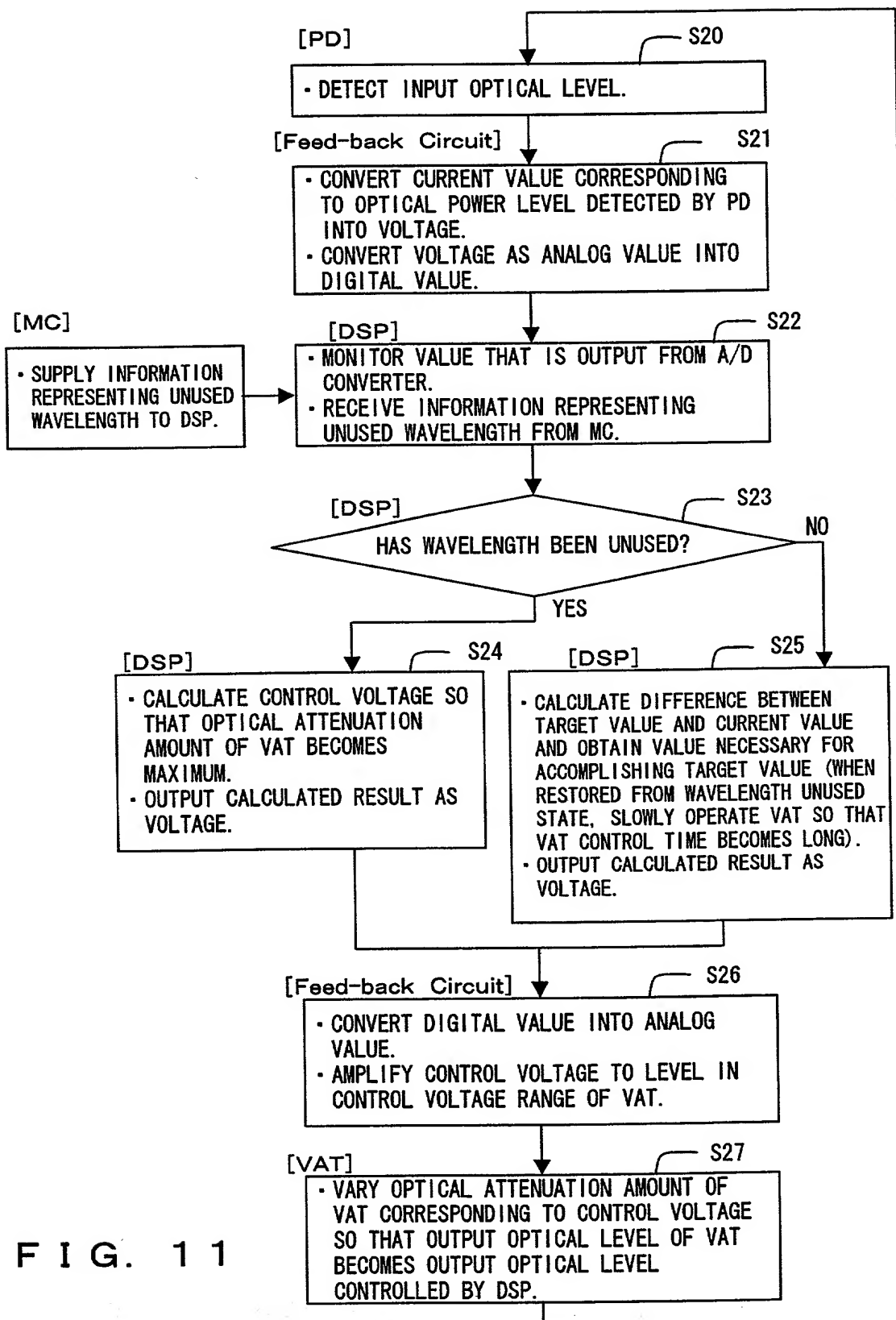


FIG. 11

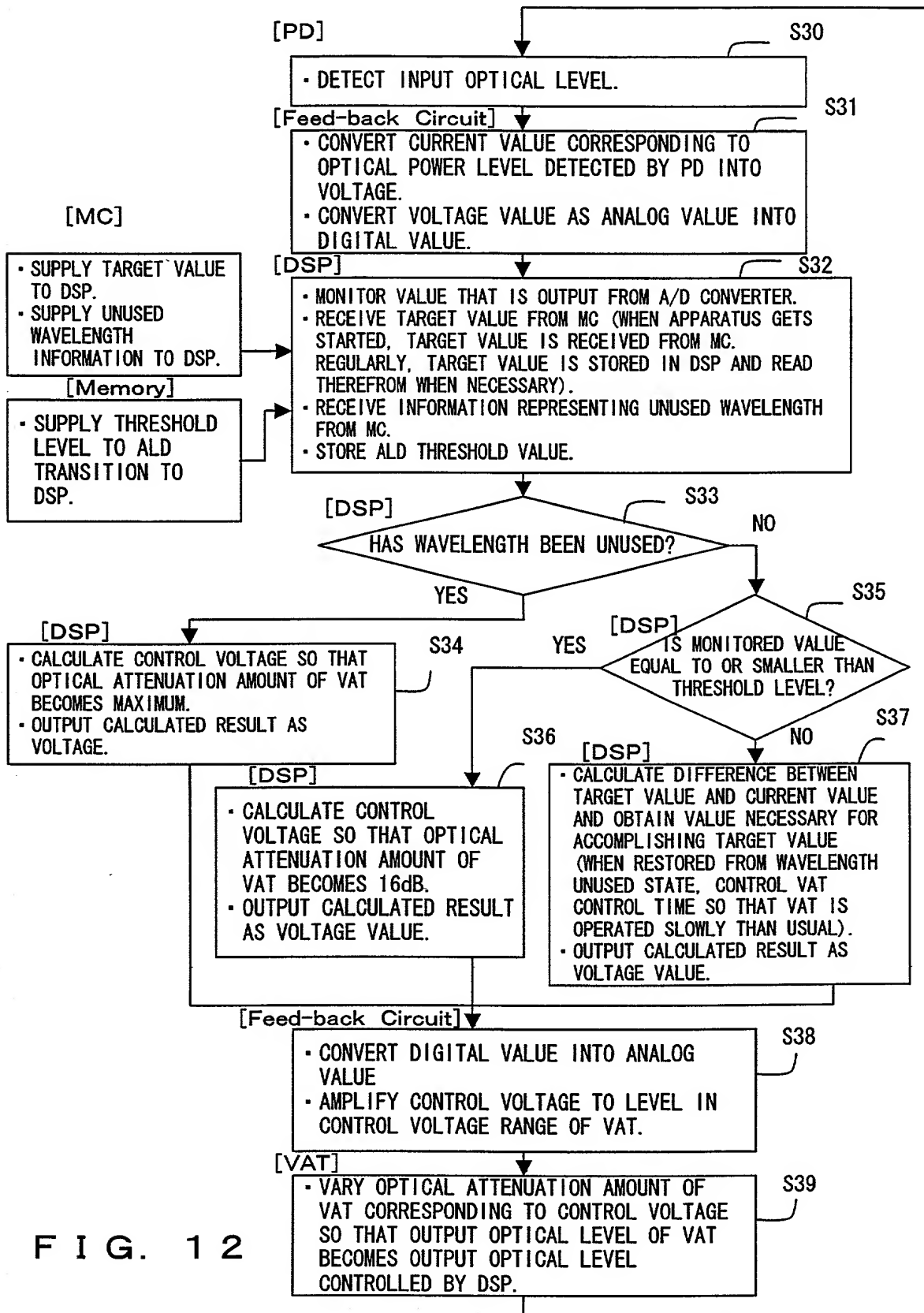


FIG. 12